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10/660,053	09/11/2003	Hideaki Takizawa	1111.68332	7258

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,053	TAKIZAWA ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35-42 and 55-62* is/are allowed.

6)☒ Claim(s) *23-34 and 43-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/669,272.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

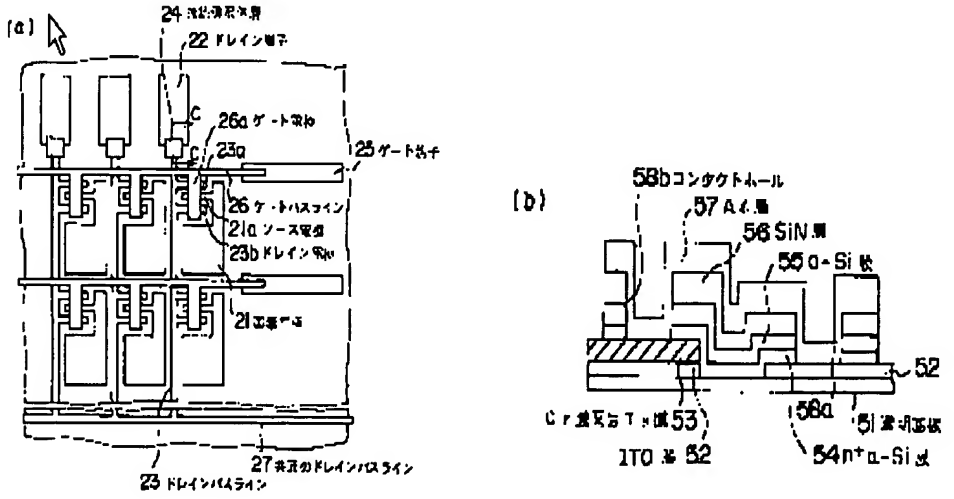
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 23-34 and 43-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirano Takuya et al. (Patent Abstracts of Japan, Publication number 07-244295, translation).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 23, **Takuya** discloses a thin film transistor matrix device comprising: an insulating substrate **51**; a plurality of thin film transistors arranged on the insulating substrate in a matrix; a plurality of picture element electrodes **21** arranged on the insulating substrate in a matrix and connected to the thin film transistors (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

a plurality of bus lines for commonly connecting the gates of the thin film transistors, the bus lines being made of a first conducting film **52**; a first insulating film formed on the first conducting film **52**; a second conducting film **53** formed on the first insulating film; and a second insulating film **56** formed on the first insulating film and the second conducting film **53** (Detailed Description, page 4, paragraph [0020] and FIGS. 1a-b); wherein, outside an image display region in which the plurality of picture elements are formed, a first contact hole **58a** is formed in the first insulating film and the second insulating film **56** through the first conducting film **52**, a second contact hole **58b** is formed in the second insulating film **56** through the second conducting film **53** (Detailed Description, paragraph, page 4, paragraph [0021] and FIGS. 1a-b);



a third conducting film **57** is formed between the first contact hole 58a and the second contact hole 58b on the second insulating film 56,

the first conducting film **52** is connected to the third connecting film **57** via the first contact hole **58a**, and

the second conducting film is connected to the third conducting film **57** via the second contact hole **58b** (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 24, **Takuya** discloses that a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 25, **Takuya** discloses that the third conducting film **57** is formed simultaneously with the plurality of picture element electrodes **21** (Detailed Description, paragraph, page 4, paragraph [0021] and FIGS. 1a-b);

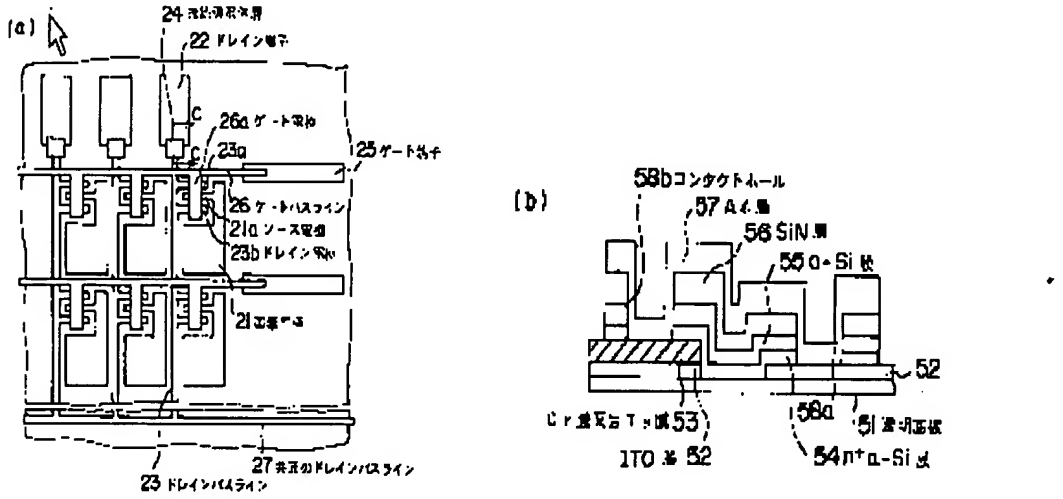
In re claim 26, **Takuya** discloses that the third conducting film **57** and the plurality of picture elements are made by Indium Tin Oxide (ITO) (Detailed Description, paragraph, page 4, paragraphs [0021]-[0022] and FIGS. 1a-b);

In re claim 27, **Takuya** discloses that the first contact hole **58a** comprises a first hole of the first insulating film and a second hole of the second insulating film **56**, and an axis of the first hole coincides with an axis of the second hole (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 28, **Takuya** discloses that the first contact hole **58a** comprises a first hole of the first insulating film and a second hole of the second insulating film **56**, and the first contact hole continues from the first hole to the second hole (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 29, **Taliua** discloses a thin film transistor matrix device comprising: an insulating substrate **51**; a plurality of thin film transistors arranged on the insulating

substrate **51** in a matrix; a plurality of picture element electrodes **21** arranged on the insulating substrate in a matrix and connected to the thin film transistors; a plurality of bus lines for commonly connecting the gates of the thin film transistors, the bus lines being made of a first conducting film **52** ((Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);



a first insulating film formed on the first conducting film **52**; a first connection line for commonly crossing the plurality of bus lines, the first connection line being made of a second conducting film **53** formed on the first insulating film; and a second insulating film **56** formed on the first insulating film and the second conducting film **53** (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

wherein, outside an image display region in which the plurality of picture element electrodes are formed, a first contact hole **58a** is formed in the first insulating film and the second insulating film through the first conducting film **52**, a second contact hole **58b** is formed in the second insulating film **56** through the second conducting film **53** (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

a third conducting film **53** is formed between the first contact hole **58a** and the second contact hole **58b** on the second insulating film,

each of the plurality of bus lines **52** is connected to the third conductive film **57** via the first contact hole **58a**, and

the first connection line **53** is connected to the third conducting film via the second contact hole **58b** (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 30, **Takuya** discloses that a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 31, **Takuya** discloses that the third conducting film **57** is formed simultaneously with the plurality of picture element electrodes **21** (Detailed Description, paragraph, page 4, paragraph [0021] and FIGS. 1a-b);

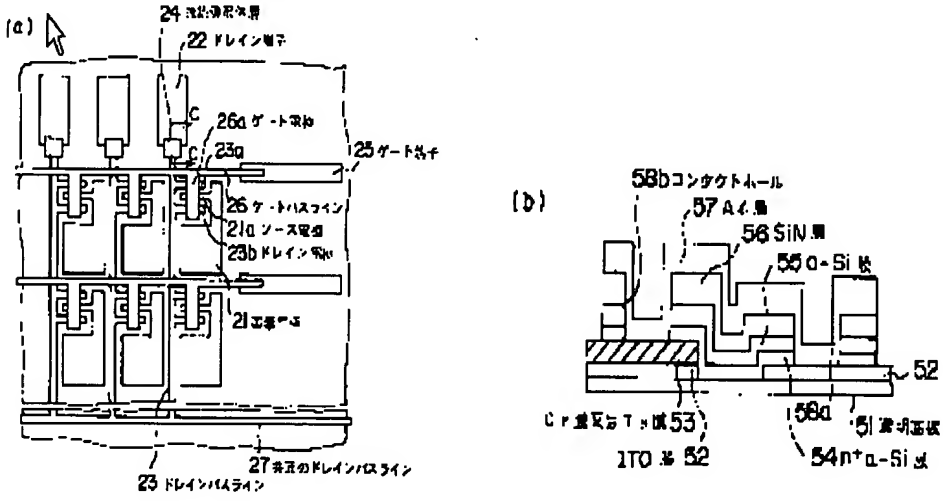
In re claim 32, **Takuya** discloses that the third conducting film **57** and the plurality of picture elements are made by Indium Tin Oxide (ITO) (Detailed Description, paragraph, page 4, paragraphs [0021]-[0022] and FIGS. 1a-b);

In re claim 33, **Takuya** discloses that the first contact hole **58a** comprises a first hole of the first insulating film and a second hole of the second insulating film **56**, and an axis of the first hole coincides with an axis of the second hole (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 34, **Takuya** discloses that the first contact hole **58a** comprises a first hole of the first insulating film and a second hole of the second insulating film **56**, and the

first contact hole continues from the first hole to the second hole (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 43, **Takuya** discloses a thin film transistor matrix device comprising: an insulating substrate **51**; a plurality of thin film transistors arranged on the insulating substrate in a matrix; a plurality of picture element electrodes **21** arranged on the insulating substrate in a matrix and connected to the thin film transistors (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);



a plurality of bus lines for commonly connecting the gates of the thin film transistors, the bus lines being made of a first conducting film **52**; a first insulating film formed on the first conducting film **52**; a second conducting film **53** formed on the first insulating film, the second conducting film **53** comprising a non-doped Silicon film, a doped n^+-type Silicon film, and a metal film; and a second insulating film **56** formed on the first insulating film and the second conducting film **53** (Detailed Description, page 4, paragraph [0020] and FIGS. 1a-b);

wherein, outside an image display region in which the plurality of picture elements are formed, a first contact hole **58a** is formed in the first insulating film and the second insulating film **56** through the first conducting film **52**, a second contact hole **58b** is formed in the second insulating film **56** through the second conducting film **53** (Detailed Description, paragraph, page 4, paragraph [0021] and FIGS. 1a-b);

a third conducting film **57** is formed between the first contact hole **58a** and the second contact hole **58b** on the second insulating film **56**,

each of the plurality of bus lines **52** is connected to the third connecting film **57** via the first contact hole **58a**, and

the first connection line is connected to the third conducting film **57** via the second contact hole **58b** (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 44, **Takuya** discloses that a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

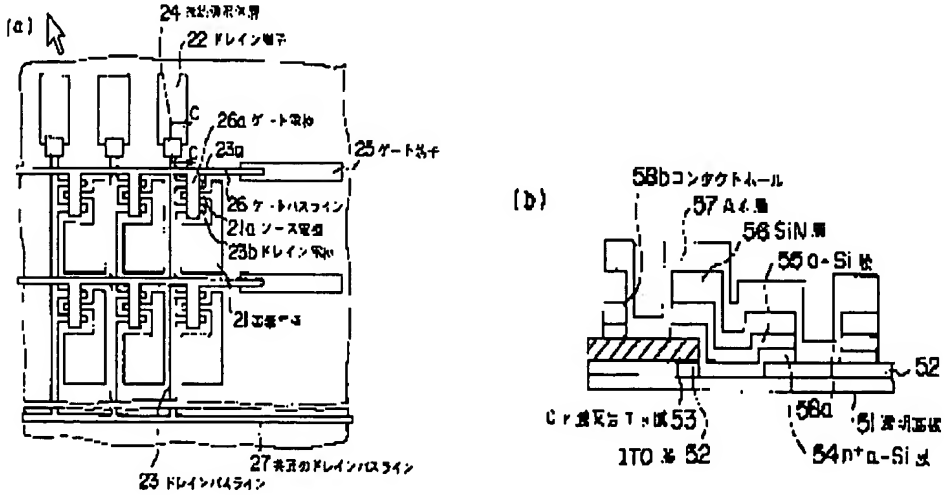
In re claim 45, **Takuya** discloses that the third conducting film **57** is formed simultaneously with the plurality of picture element electrodes **21** (Detailed Description, paragraph, page 4, paragraph [0021] and FIGS. 1a-b);

In re claim 46, **Takuya** discloses that the third conducting film **57** and the plurality of picture elements are made by Indium Tin Oxide (ITO) (Detailed Description, paragraph, page 4, paragraphs [0021]-[0022] and FIGS. 1a-b);

In re claim 47, **Takuya** discloses that the first contact hole **58a** comprises a first hole of the first insulating film and a second hole of the second insulating film **56**, and an axis of the first hole coincides with an axis of the second hole (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 48, **Takuya** discloses that the first contact hole **58a** comprises a first hole of the first insulating film and a second hole of the second insulating film **56**, and the first contact hole continues from the first hole to the second hole (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 49, **Takuya** discloses a thin film transistor matrix device comprising: an insulating substrate **51**; a plurality of thin film transistors arranged on the insulating substrate in a matrix; a plurality of picture element electrodes **21** arranged on the insulating substrate in a matrix and connected to the thin film transistors (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);



a plurality of bus lines for commonly connecting the gates of the thin film transistors, the bus lines being made of a first conducting film **52**; a first insulating film formed on the first conducting film **52**;

a first connection line **53** for commonly crossing the plurality of bus lines **52**, the first connection line being made of a second conducting film formed on the first insulating film, the second conducting film **53** comprising a non-doped Silicon film, a doped n^+-type Silicon film, and a metal film; and a second insulating film **56** formed on the first insulating film and the second conducting film **53** (Detailed Description, page 4, paragraph [0020] and FIGS. 1a-b);

wherein, outside an image display region in which the plurality of picture elements are formed, a first contact hole **58a** is formed in the first insulating film and the second insulating film **56** through the first conducting film **52**, a second contact hole **58b** is formed in the second insulating film **56** through the second conducting film **53** (Detailed Description, paragraph, page 4, paragraph [0021] and FIGS. 1a-b);

a third conducting film **57** is formed between the first contact hole **58a** and the second contact hole **58b** on the second insulating film **56**,

each of the plurality of bus lines **52** is connected to the third connecting film **57** via the first contact hole **58a**, and

the first connection line is connected to the third conducting film **57** via the second contact hole **58b** (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 50, **Takuya** discloses that a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 51, **Takuya** discloses that the third conducting film **57** is formed simultaneously with the plurality of picture element electrodes **21** (Detailed Description, paragraph, page 4, paragraph [0021] and FIGS. 1a-b);

In re claim 52, **Takuya** discloses that the third conducting film **57** and the plurality of picture elements are made by Indium Tin Oxide (ITO) (Detailed Description, paragraph, page 4, paragraphs [0021]-[0022] and FIGS. 1a-b);

In re claim 53, **Takuya** discloses that the first contact hole **58a** comprises a first hole of the first insulating film and a second hole of the second insulating film **56**, and an axis of the first hole coincides with an axis of the second hole (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

In re claim 54, **Takuya** discloses that the first contact hole **58a** comprises a first hole of the first insulating film and a second hole of the second insulating film **56**, and the first contact hole continues from the first hole to the second hole (Detailed Description, paragraph, page 4, paragraph [0020] and FIGS. 1a-b);

Allowable Subject Matter

Claims 35-42 and 55-62 are allowed.

Response to Applicant's Amendment and Arguments

Applicants' arguments with respect to claims 23-34 and 43-54 have been considered but are moot in view of the new ground(s) of rejection.

Applicants contend that the Ikeda et al. (U.S. Patent 5,182,661) fails to include the first and second contact holes and the first, second and third conducting films, which are all formed "outside an image display region in which the plurality of picture element electrodes are formed," as defined in independent Claims 23, 29, 43, and 49.

In response to Applicants' contention that Ikeda et al. fail to include the first and second contact holes and the first, second and third conducting films, which are all formed "outside an image display region in which the plurality of picture element electrodes are formed," as defined in independent Claims 23, 29, 43, and 49, Examiner respectfully submits that Applicants' argument is moot in view of the newly discovered reference to Hirano Takuya et al. (Patent Abstracts of Japan, Publication number 07-244295, translation) applied under 35 U.S.C. 102(e) new ground of rejection presented in this Office Action.

For this reason, Examiner holds the rejection proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
August 17th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER